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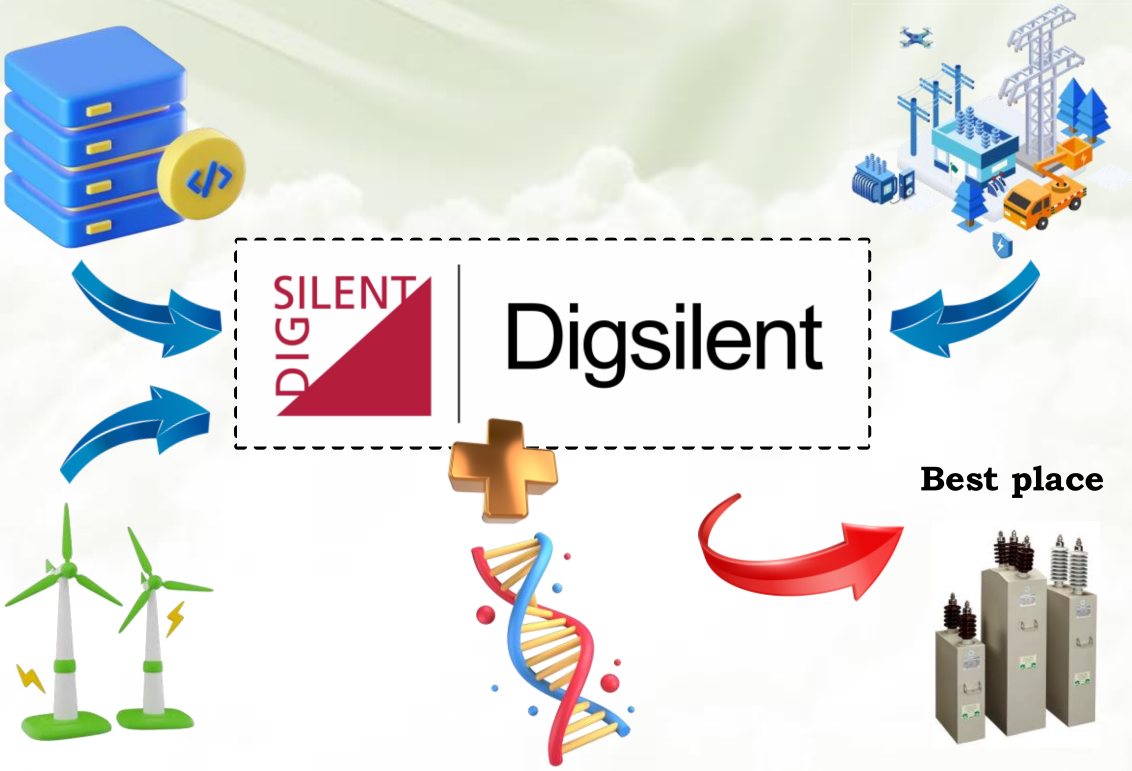
Highlight

- **Minimize losses while meeting voltage and harmonic constraints is proposed**
- **Proper capacitor size and location selection to improve voltage deviations with low harmonics is suggested.**
- **Optimally-sized and located parallel capacitors reduce losses, improve voltage profile and stability, and address issues with inductive loads.**

Graphical Abstract



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Optimal Capacitor Placement in Distributed Networks Polluted with Harmonics in the Presence of Wind Energy-based Distributed Generation Sources

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ABSTRACT

In electrical distribution networks, inefficiencies and instabilities often arise from inductive loads like motors and transformers, which exhibit a lagging power factor. This reduces system capacity, increases losses, and can lead to lower voltage levels. To address these issues, integrating parallel capacitors proves effective, enhancing the power factor, improving voltage profiles, and reducing overall system losses and costs. This research explores the optimal placement of parallel capacitors within a distribution network to manage reactive power effectively, thereby minimizing losses and improving voltage stability and system efficiency. Utilizing DigSILENT Power Factory and MATLAB, a genetic algorithm optimizes the location and sizing of capacitors in a 33-bus distribution network, considering scenarios with and without distributed generation (DG) and the impact of harmonic currents.

The study finds that incorrect sizing or placement of capacitors can worsen voltage deviations when higher harmonic levels are present. However, the optimization method accurately determines the best parameters for capacitor installation, ensuring compliance with voltage and harmonic constraints. Deploying more than three to four capacitors does not significantly affect outcomes, while a single busbar capacitor often fails to meet operational standards. In conclusion, strategic capacitor placement and sizing can significantly reduce losses, enhance voltage stability, and mitigate inefficiencies caused by inductive loads. Attention to harmonics is crucial to avoid negative impacts on the network. This approach offers a replicable framework for similar optimizations in other distribution systems, advancing smart grid technology implementation.

1. Introduction

The integration of wind turbine DGs into the electrical grid represents a sustainable energy advancement, albeit accompanied by significant technical challenges. Notably, the power converters within these turbines are sources of harmonic distortion that may jeopardize grid stability and damage electrical equipment [1]. Harmonics can be conceptualized as undesirable electrical "noise" that interferes with the seamless flow of power, analogous to static on a radio signal. The severity of this distortion is influenced by multiple factors such as the type of converter, its control mechanisms, and the inherent robustness of the grid [2, 3]. A weak grid, akin to a fragile clothesline, might sustain light winds (low wind power) but could falter under strong gusts (high wind power), leading to instability. Additionally, the intrinsic variability of wind energy contributes to further challenges, as inconsistent wind speeds can lead to fluctuations in grid frequency and voltage [4].

The issue of optimal capacitor placement within distribution systems has also garnered considerable attention due to the diverse benefits that capacitors offer, including reduction in power losses [5], enhancement of voltage profiles, augmentation of system capacity and reliability, and improvement of power factor. To address this complex problem, a variety of analytical, heuristic, and metaheuristic methods have been employed to effectively site and size capacitors. Early research efforts centered on articulating the core problem using simplified system models and constraints [5-7]. Sensitivity analyses were employed to pinpoint potential capacitor locations [5], and methods such as gravitational search algorithms were utilized to determine near-optimal capacitor sizes. Additionally, innovative heuristic techniques based on interior point nonlinear programming relaxation have been developed to swiftly identify high-potential buses for capacitors [6].

Further advances have seen the integration of analytical screening with metaheuristic global search strategies, such as the use of loss sensitivity factor analysis for selecting capacitor sites and ant colony optimization for determining optimal sizes [7]. These hybrid methodologies have effectively narrowed the search space, yielding high-quality solutions. Moreover, various metaheuristic approaches tailored for the capacitor placement challenge have been proposed, including particle swarm optimization [8], simulated annealing [9], genetic algorithms [10], discrete particle swarm optimization [11], ant colony search [12], clustering-based optimization [13], and teaching-learning-based optimization [14]. Despite their intensive computational demands, these methods are adept at handling complex, nonconvex constraints across extensive, multidimensional solution spaces.

Recent research has increasingly focused on integrating practical considerations into problem formulations, such as the incorporation of existing capacitors, discrete capacitor sizes, time-varying loads, harmonics, and the costs associated with installation and operation [15]. Other considerations include reliability indices [16], voltage regulation [17], loss reduction [18], and multiobjective trade-offs [19]. Advanced power flow analysis techniques, such as backward/forward sweep and radial distribution power flow, have been pivotal in evaluating complex problem formulations under realistic operating conditions. Test scenarios range from standard IEEE benchmark systems with 13 and 33 buses to large-scale distribution networks with over 200 buses, demonstrating the effectiveness of optimized approaches on extensive operational infrastructures.

In sum, the quality of electricity delivery is generally assessed by ensuring that frequency, waveform, and voltage level parameters remain within standardized and acceptable limits. Disturbances or harmonic effects primarily manifest through voltage harmonics, although harmonic currents can also induce issues like telephone interference and may influence the network remotely [20]. Although the frequency of electricity supplied by power plants is controllable and unaffected by consumers, the waveform and voltage levels are directly influenced by the loads within the network, especially nonlinear loads that introduce harmonics [21].

This research develops an advanced optimization framework for strategically placing capacitors in distributed networks, particularly those integrating wind energy-based DG sources and experiencing harmonic distortions. The study introduces a multi-objective optimization problem, targeting both power loss reduction and voltage profile enhancement, while also considering voltage limits and harmonic levels. A genetic algorithm, implemented in DigSILENT software, is employed to address this complex problem, enabling detailed evaluation of various scenarios including those without DGs or harmonic impacts, and others focusing solely on loss reduction or voltage improvement.

The evaluation highlights the crucial role of harmonics in capacitor placement. It finds that incorrect capacitor sizing or location can lead to worse voltage deviations when harmonics are present, underscoring the need for incorporating harmonic mitigation in the optimization process. Additionally, the study establishes that installing more than three to four capacitors offers diminishing returns in a 33-bus test system, providing practical insights for system operators on the limits of capacitor utility.

The paper is organized into several sections: Section 1 provides an introduction, background, and motivation for the research; Section 2 details the formulation of the optimization problem, including definitions of variables, objective functions, and constraints; Section 3 describes the solution methodology using a genetic algorithm and the software tools employed; Section 4 discusses the results of simulations under various scenarios, including those without DGs/harmonics and those focusing on loss or voltage profiles, as well as scenarios incorporating DGs/harmonics. Finally, Section 5 summarizes the key findings and conclusions of the study.

2. Problem formulation

2.1. Optimization problem variables

The variables of the optimization problem include the size of capacitor units, the maximum number of capacitor units that can be installed at each busbar or node, and the maximum number of busbars or nodes considered for capacitor placement.

2.2. Objective function

The objective function of this program is to reduce losses and improve the voltage profile. Although users can also input their desired objective function, voltage, and harmonic constraints are added to the objective function by large penalty coefficients.

2.3. Optimization problem constraints

The constraints of the optimal capacitor placement problem include the permissible voltage range of busbars, the maximum loading limit of distribution network lines, and the permissible harmonic range of voltage at network busbars. If the capacitor is installed at the consumer's location, the power loss reduction after installation in the feeder is obtained from Equation (1):

$$LR = R[2I_L(RLF)I_c - I_C^2] \tag{1}$$

In this equation, (I_L) represents the load current, (I_C) denotes the capacitor current, and (RLF) is the reactive load factor. Reducing losses has the following advantages:

- Reduction of maximum load (demand) losses
- Energy savings thanks to energy loss reduction
- Reduction of maximum reactive load
- Voltage improvement

By employing capacitors in a system, an increase in system voltage will be achieved from the installation to the generation points. In a system with a leading power factor, the voltage increases because capacitors can reduce the reactive current transfer of the system. As a result, the reactive and resistive voltage drop in the system decreases [22]. Several formulae are available to estimate the voltage increase caused by capacitors, but typically the following formula is used:

$$\Delta V = \frac{(Kvar)(X_1)}{10(kv)^2} \tag{2}$$

ΔV: The amount of voltage increase at capacitor point
kv: Line-to-line voltage of the system without using a capacitor
$Kvar$: Three-phase nominal reactive power of the capacitor bank
X_1: Inductive reactance of the system at the place of installation of the capacitor, Ohm

Voltage constraint can be expressed as in Equation (3):

$$V_{min} \leq V_i \leq V_{max}: i = 1 \ldots N_n \tag{3}$$

N_n is the number of buses or nodes.

The condition of the allowed line currents can be expressed as follows in Equation (4):

$$I_{min} \leq I_j \leq I_{max}: j = 1 \ldots N_b \tag{4}$$

Where N_b is the number of lines or branches.

3. Solution methodology

3.1. Genetic algorithm

In this study, a genetic algorithm and DigSILENT are used. The algorithm is a random search method based on natural selection. This algorithm consists of a population, where each individual in the population (chromosomes) represents a sample solution, and each component of the chromosomes (genes) represents a specific variable of the problem. A new generation is produced by considering the fitness function of individuals and using genetic operators (crossover and mutation), and the fitness function improves over the iterations of the algorithm [23].

In the first step of solving the problem, a random population is used. The genetic algorithm improves the initial population by applying operators on chromosomes and provides it to the next generation. These operators include evolution, crossover, mutation, and shuffling. Through the evolution operator, chromosomes with the highest fitness in each generation are selected and sent to the next generation. Exchange of multiple points is performed among the chromosomes that have reached the previous generation, such that a certain percentage of similar genes between two parent chromosomes are randomly selected and exchanged, creating two new chromosomes. As a result, no defective chromosomes are created due to the crossover operation [24].

A mutation is performed on a limited number of random bits of the chromosomes that have reached the previous generation, and these bits are randomly changed to new, random numbers. This way, the likelihood of the optimization algorithm getting stuck in local optimum points is reduced. In this study, the genetic algorithm available in the MATLAB software is used.

3.2. Software packages

In this work, DigSILENT software is used, and communication with MATLAB is established through a DigSILENT programming language (DPL) program. Initially, the MATLAB program is executed, which receives initial information, including the number of candidate busbars for capacitor locations, the number of considered busbars, and the size of capacitor units, from the user. Then, the genetic algorithm is invoked. After receiving the capacitor placement vector containing the location and size of capacitors, it calls the second DPL file.

In this file, the capacitor placement vector is exported to DigSILENT in the form of a data file and waits for the response. After receiving the software response, which includes the value of the objective function, the results are stored for the next iteration in the first DPL file.

After receiving the file containing the information about the location and size of capacitors in the software, it performs capacitor placement in the network, calculates the objective function, and sends it to MATLAB. The objective function of this program is to reduce losses while considering voltage and harmonic constraints. Although the user can also input their desired objective function, voltage, and harmonic constraints are added to the objective function by large penalty coefficients. This approach ensures that the genetic algorithm distances itself from capacitor placement in busbars that may lead to severe voltage drop or worse harmonic conditions.

The second DPL is used to calculate losses. This program calculates losses and the objective function after optimal capacitor placement. It is worth mentioning that in the DigSILENT software, the total network losses or losses of individual lines are not calculated in the presence of harmonics. Therefore, these calculations need to be programmed. Figure 1 shows the flowchart of problem-solving steps.

4. Simulation and results

4.1. Base case analysis

In this section, simulation results of optimal capacitor placement in a standard distribution network are presented. The set of software and developed programs is capable of determining the location and number (size) of capacitor banks for a hypothetical network with harmonics in a way that minimizes the objective function. The objective function is a combination of user-defined coefficients for losses and voltage profiles.

The network under study is a standard IEEE 33-bus distribution network with a base voltage of 11 kV. The linear single-line diagram of the IEEE 33-bus network and the locations of each busbar are illustrated in Figure 2.

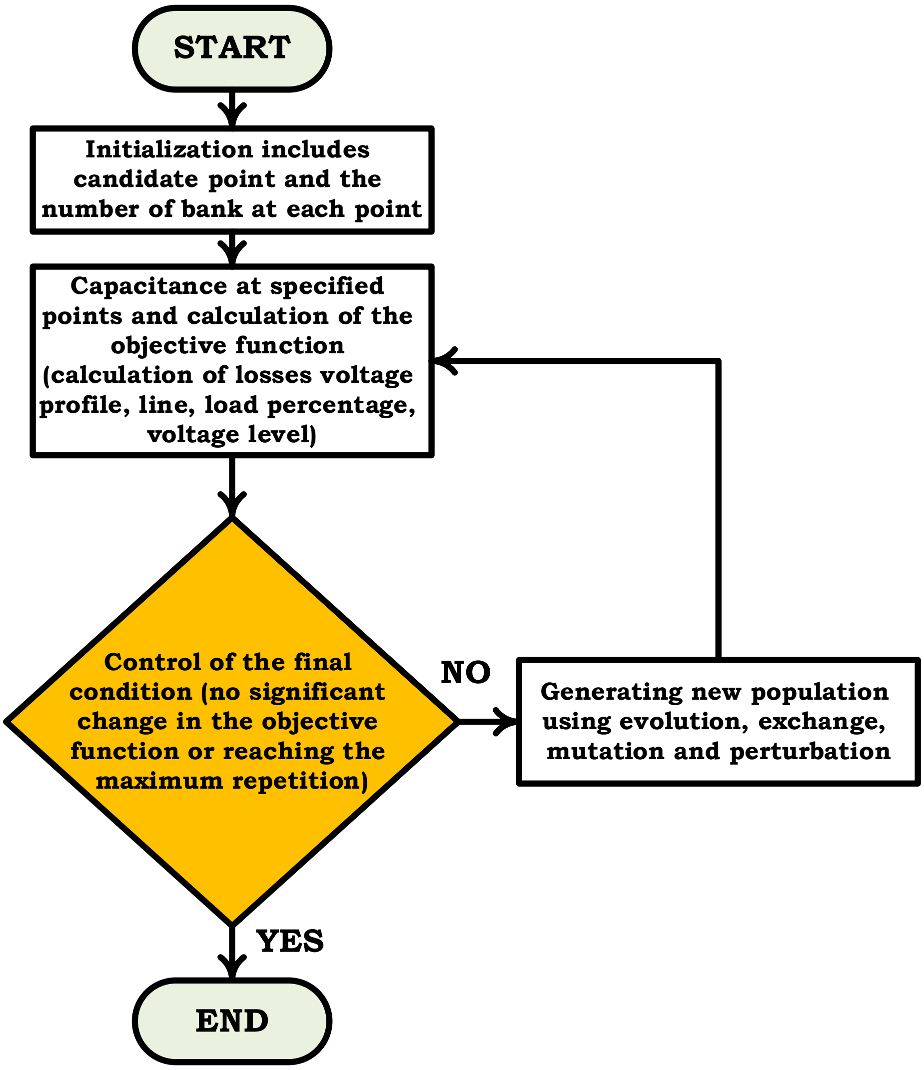


Figure 1. The flowchart of problem-solving steps.

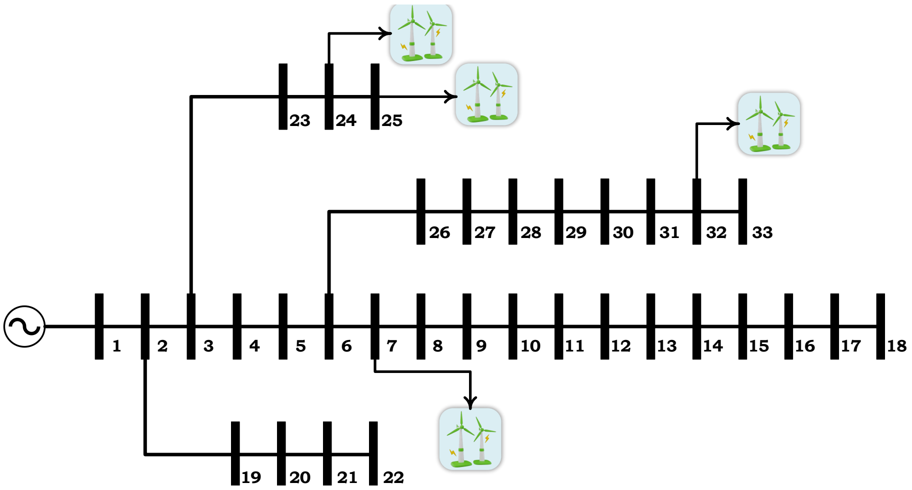
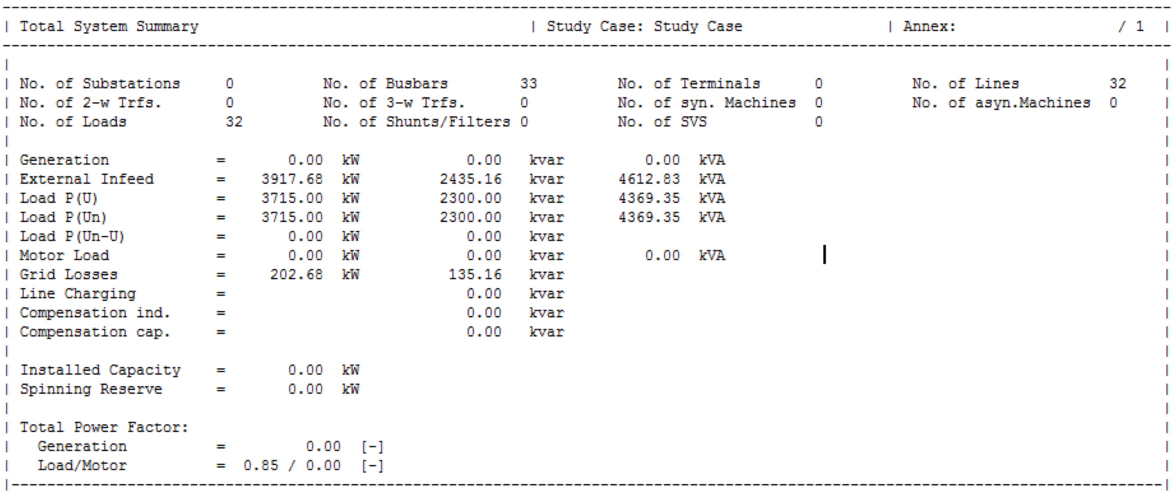


Figure 2. Single-line view of the 33-bus network.



```
------------------------------------------------------------------------------------------------------------------------------
| Total System Summary                                        | Study Case: Study Case                 | Annex:                / 1  |
------------------------------------------------------------------------------------------------------------------------------
|                                                                                                                            |
| No. of Substations     0          No. of Busbars        33          No. of Terminals      0          No. of Lines          32  |
| No. of 2-w Trfs.       0          No. of 3-w Trfs.      0           No. of syn. Machines  0          No. of asyn.Machines  0   |
| No. of Loads           32         No. of Shunts/Filters 0           No. of SVS            0                                     |
|                                                                                                                            |
| Generation            =       0.00  kW            0.00   kvar        0.00  kVA                                           |
| External Infeed       =    3917.68  kW         2435.16   kvar     4612.83  kVA                                           |
| Load P(U)             =    3715.00  kW         2300.00   kvar     4369.35  kVA                                           |
| Load P(Un)            =    3715.00  kW         2300.00   kvar     4369.35  kVA                                           |
| Load P(Un-U)          =       0.00  kW            0.00   kvar                                                            |
| Motor Load            =       0.00  kW            0.00   kvar        0.00  kVA           |                               |
| Grid Losses           =     202.68  kW          135.16   kvar                                                            |
| Line Charging         =                           0.00   kvar                                                            |
| Compensation ind.     =                           0.00   kvar                                                            |
| Compensation cap.     =                           0.00   kvar                                                            |
|                                                                                                                            |
| Installed Capacity    =       0.00  kW                                                                                     |
| Spinning Reserve      =       0.00  kW                                                                                     |
|                                                                                                                            |
| Total Power Factor:                                                                                                        |
|   Generation          =         0.00  [-]                                                                                  |
|   Load/Motor          =  0.85 / 0.00  [-]                                                                                  |
|----------------------------------------------------------------------------------------------------------------------------|
```

Figure 3. Summary of the standard 33-bus network.

In this study, the standard distribution network is modelled in DigSILENT Power Factory software. Additionally, MATLAB software is used for optimization calculations and the genetic algorithm. A program is written in the DPL to establish communication between the network and the genetic algorithm. A summary of the standard network report is shown in Figure 3. As illustrated, the total losses of the network are equal to 202.68 kW.

To consider the effects of DG and harmonics resulting from nonlinear loads, the following modifications, according to reference [25], were applied to the standard network. These modifications include adding DG at busbars 7, 24, 25, and 32, and replacing the existing linear load with a nonlinear (harmonic) load at busbars 6 and 27.

Simulation results indicate that in the first stage, with the introduction of DG and a total generation of 800 kW, network losses decrease to 172.8 kW. In the next stage, with an increase in load, network losses increase to 510.45 kW. To consider the effects of harmonics, according to Table 1, the harmonic model of the six-pulse converter was added to DG and nonlinear loads. The harmonics of the six-pulse converter are illustrated in Figure 4. The network losses with harmonics present will be 518.18 kW, indicating an increase of 8 kW compared to the harmonic-free condition.

Table 1. Test network changes compared to the standard network**.**

Type of change	Type of Harmonic	Q (kVar)	P (kW)	Busbar No.
Adding a DG	6 pulse converter	97	200	7
	6 pulse converter	97	200	24
	6 pulse converter	97	200	25
	6 pulse converter	97	200	32
Alternative Load	6 pulse converter	750	1000	6
	6 pulse converter	750	1000	27

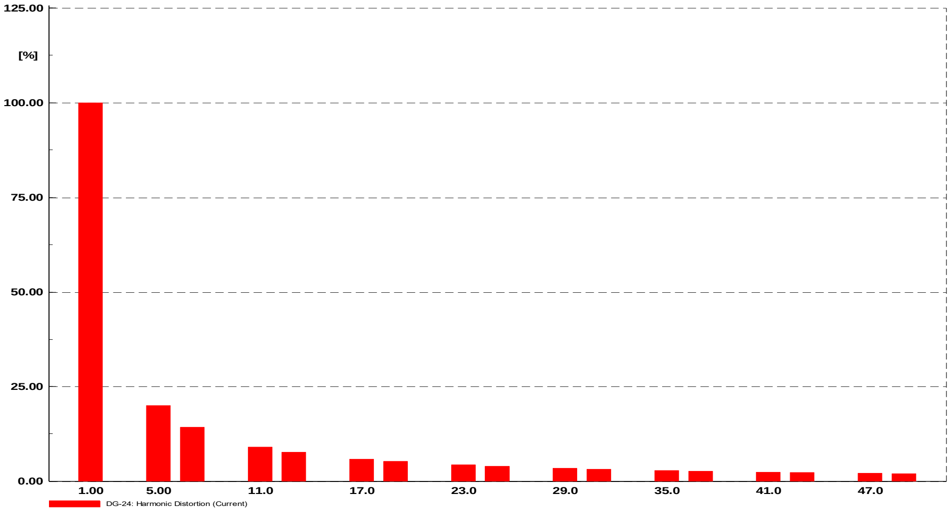
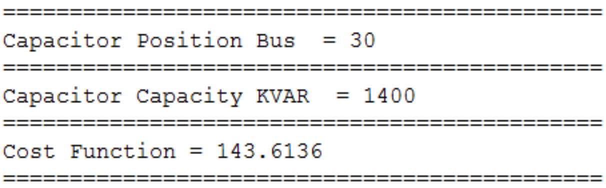


Figure 4. Spectrum of current harmonics of six-pulse converter**.**



```
============================================
Capacitor Position Bus  = 30
============================================
Capacitor Capacity KVAR  = 1400
============================================
Cost Function = 143.6136
============================================
```

Figure 5. Sample output of a MATLAB program for a capacitor-compensated busbar.

To place capacitors using the genetic algorithm, MATLAB software has been employed. For program execution, the number of candidate capacitor busbars and the size of capacitor units are specified as inputs. In this study, simulations were performed assuming 1 to 4 capacitor busbars.

4.2. Capacitor placement without harmonic load

Without considering harmonic loads and DG, capacitor placement is performed to reduce losses and improve voltage profile. In the first stage, capacitor placement is done solely with the objective of loss reduction. The output of the program is illustrated in Figure 5. Therefore, if there is one candidate busbar capacitor with the loss reduction objective, then busbar number 30, with a size of 1400 kVA, will be the optimal busbar. In this case, network losses will decrease from 202.68 kW to 143.6 kW. The complete results are shown in Table 2. Each of the solutions converged to an answer after approximately 6000 iterations.

Next, capacitor placement to improve the voltage profile has been carried out. In this case, the percentage of voltage drop or rise in all network busbars has been selected as the objective function. A decrease in this value implies that the voltage at busbars is approaching unity. The results of running the program are shown in Table 3.

According to Figure 6, using the objective function to improve the voltage profile (reduce the distance of voltages from unity) has been achieved successfully through capacitor placement. However, a crucial point to consider is the comparison of network losses before and after capacitor placement. The network losses with this capacitor placement approach have reached approximately 540 kW, showing an increase close to 170% compared to network losses without capacitors. Therefore, it can be concluded that the voltage index alone may not be sufficient.

Table 2. Capacitor placement for loss reduction in test network without dg and harmonic loads.

Number of candidate busbars for capacitor placement	Losses (kW)	Total capacitance placement (kVAR)	Capacitance placement per busbar in each order (kVAR)	Capacitor-placed busbars
0	68/202	0	-	-
1	6/143	1400	1400	30
2	7/135	1700	550-1150	11-30
3	2/132	2150	550-500-1100	24-13-30
4	2/132	2150	1000-500-250-400	5-24-12-30

Table 3. Results of capacitor placement for voltage profile improvement in test network without DG and harmonic loads.

Number of candidate busbars for capacitor placement	Voltage profile index	Total capacitance placement (kVAR)	Capacitance placement per busbar in each order (kVAR)	Capacitor-placed busbars
0	1/170	0	-	-
1	5/45	5000	5000	8
2	7/14	5850	1500-4350	13-28
3	4/12	8490	3650-2300-2450	12-24-30
4	0/9	7900	1650-4250-1100-900	25-26-31-16

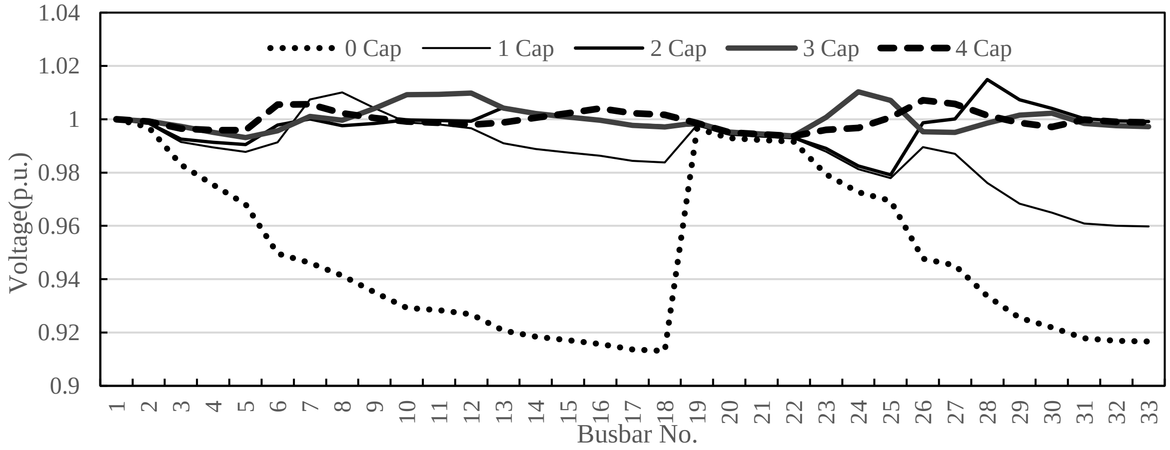


Figure 6. Standard network bus voltages after capacitor placement to improve voltage profile.

Considering that the proximity of busbar voltages can create a good margin of confidence for network utilization, it is possible to use the sum of two indices, losses, and voltage profile, for optimal capacitor placement. It should be noted that in some research, the voltage placement index within the normal range (0.5 to 0.95 per unit (p.u.)) has been considered as the voltage share in the objective function. This index, considering load variations, will not provide a suitable safe range for the operator. In Table 4, simulation results considering both loss and voltage indices simultaneously are presented.

As shown in Figure 7, considering the objective function with a combined index, in addition to reducing losses, the voltage is also within the permissible range (above 0.95 p.u.). In this case, network losses amount to 145 kW, which is a reduction compared to the base case (202 kW). In Figure 7, the voltage profile status is depicted for two scenarios with the objective function of loss index and the objective function of voltage index.

Table 4. Results of capacitor placement to reduce losses and improve voltage profile in the test network without the presence of DG and harmonic loads.

Number of candidate busbars for capacitor placement	Total index (losses + 100 times the sum of voltage deviations)	Total capacitance placement (kVAR)	Capacitance placement per busbar in each order (kVAR)	Capacitor-placed busbars
0	8/372	0	-	-
1	9/291	3750	3750	7
2	244	2300	800-1500	14-30
3	9/235	2800	1150-500-1150	7-30-14
4	8/232	3250	600-900-1200-550	24-7-30-14

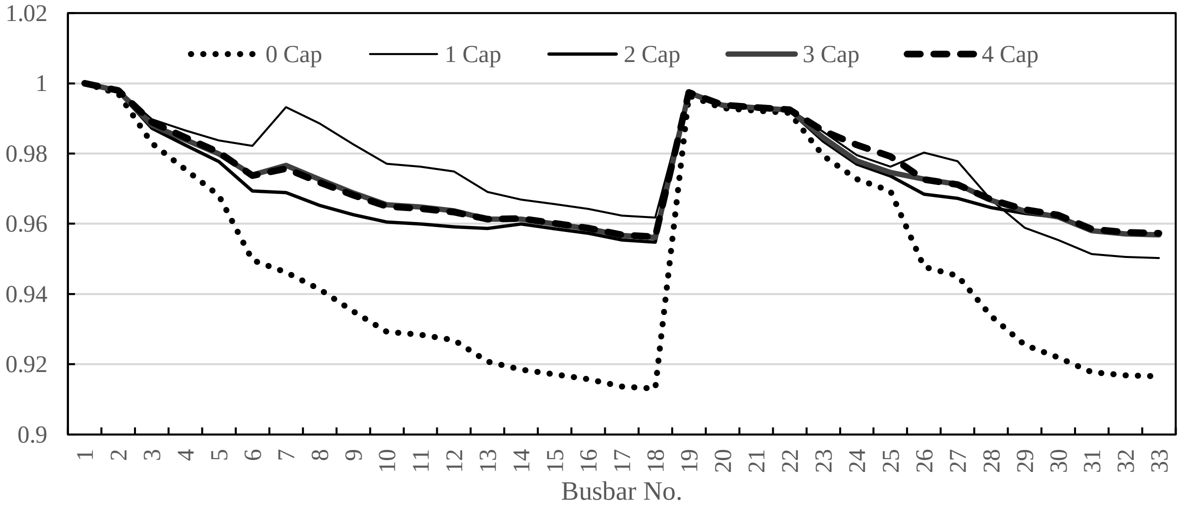


Figure 7. Comparison of bus voltages to simultaneously reduce losses and improve voltage profile in the standard network.

4.3. Capacitor placement with harmonic loads and DG

Taking harmonic loads into account in the network, harmonic reduction can be added to other capacitor placement objectives. If capacitor placement is done incorrectly in a harmonic-rich network, it can worsen harmonic distortion conditions. For example, Figure 8 shows the result of incorrectly placing a capacitor in the test network at only 50 kW at busbar number 6. As illustrated, harmonic distortion has significantly increased after capacitor placement. In practice, such a situation can lead to the fuse of the capacitor bank burning out.

The occurrence of intensification is near harmonic number 49. Also, the change in the behavior of the impedance observed from busbar number 6 with the presence of 50, 100, and 1000 kVar capacitor banks in this busbar, based on the change in the frequency coefficient, is shown.

Given the mentioned content, it can be concluded that capacitor placement in harmonic networks should be done with precision and sufficient study. Therefore, reducing harmonic distortion can also be added to the objective function of optimal capacitor placement. Considering the direct relationship between losses and harmonics, if the objective function is chosen as losses, it is expected that harmonic distortion in the network will decrease. Thus, the level of harmonic distortion and bus voltages can be considered as constraints, and the objective function can be selected as losses. Table 5 presents the results of optimal capacitor placement to reduce losses, with a constraint on voltage drop or increase not exceeding 5% and a maximum overall voltage distortion of 5%.

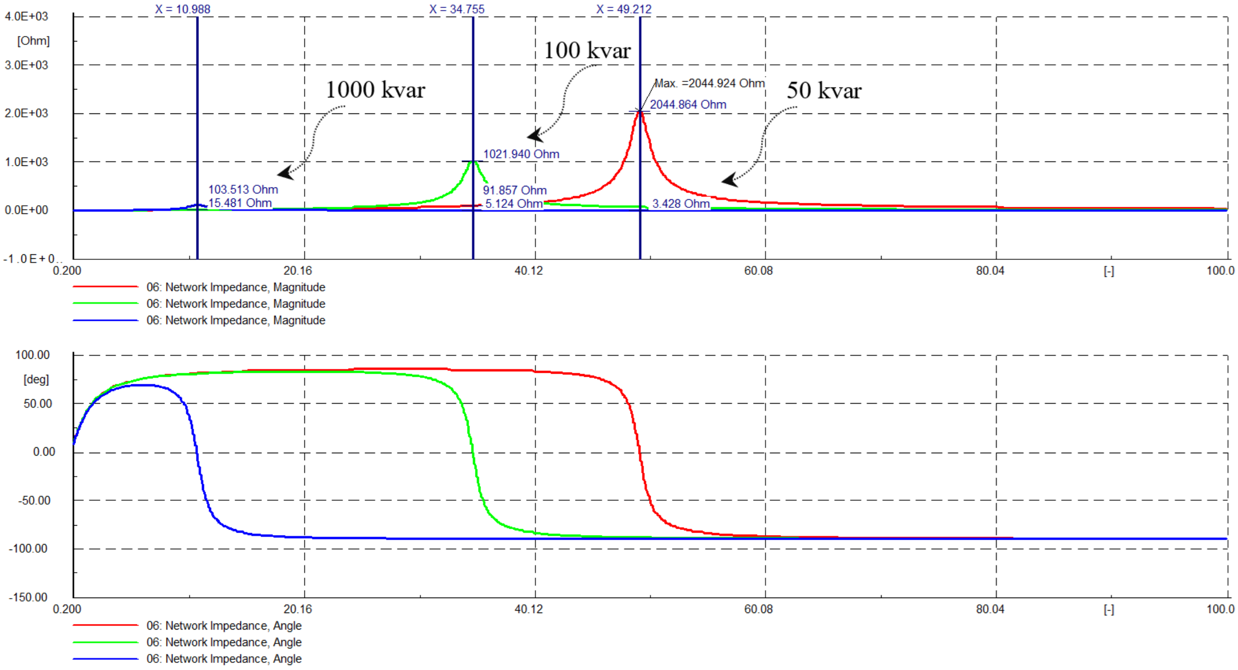


Figure 8. Frequency scan of the impedance of bus No. 6 for various capacitor sizes.

The examination of Table 5 indicates that using a single capacitor bank does not provide the possibility of reducing losses. However, employing two or more capacitors for installation can reduce losses in the harmonic network. The voltage and harmonic status of the capacitors are illustrated in Figures 9 and 10, respectively. As shown in Figure 9, it was not possible to meet the voltage constraint in buses 26 to 33 using a single capacitor. In other cases (utilizing more than one capacitor), the voltage constraint has been achieved. The results in Figure 10 demonstrate that, despite having a single capacitor for capacitive placement, the reduction of total voltage distortion in buses 26 to 33 was not feasible.

Table 5. Capacitor placement to reduce losses and constraints on harmonic distortion in the presence of DG.

Number of candidate busbars for capacitor placement	Total Losses Index (kW)	Total capacitance placement (kVAR)	Capacitance placement per busbar in each order (kVAR)	Capacitor-placed busbars
0	18/518	0	-	-
1	17/558	4750	4750	9
2	400	5050	2800-2250	11-29
3	5/347	5350	2350-1050-1950	30-13-7
4	6/325	5000	800-1400-2050-750	15-32-7-29

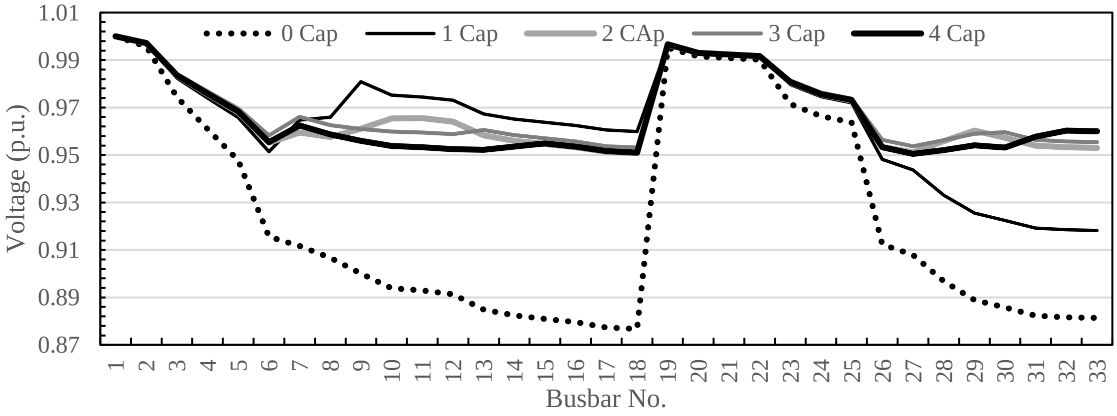


Figure 9. Busbar voltages to reduce losses and constraints on voltage and harmonic distortion.

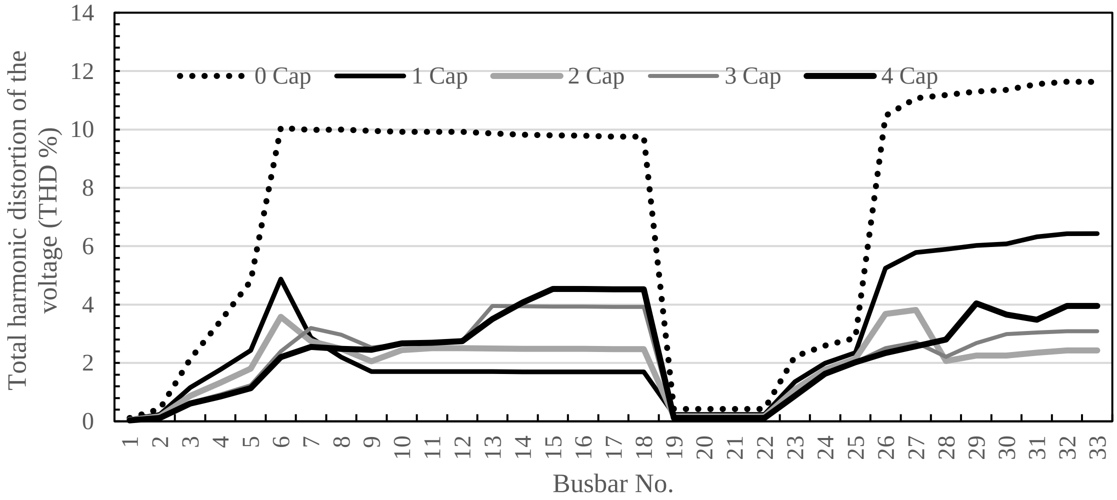


Figure 10. Total voltage distortion in network busbars with the presence of harmonic sources and DG.

However, in other capacitor placement scenarios, the overall voltage distortion remained below the standard limit (5%). Simulation results in this study have been compared with the reference [25], and the comparison is presented in Table 6.

5. Conclusion

The key achievements and findings from this study on the optimal placement of capacitors in distributed networks, particularly those incorporating wind energy-based DGs and experiencing harmonic distortions, are significant. Notably, the study found that when harmonic loads were not considered, optimization could effectively reduce network losses by up to 33% compared to baseline scenarios. However, targeting capacitors solely to enhance voltage profiles led to increased network losses, underscoring the necessity of integrating both loss reduction and voltage stabilization in the optimization objectives.

Employing a combined index objective function that addressed both losses and voltage deviations enabled the optimization to secure a 28% reduction in losses while maintaining voltage levels above 0.95 p.u. This highlights the effectiveness of a multi-objective approach in achieving comprehensive system enhancements. In scenarios involving harmonic-generating loads and wind-based DGs, inappropriate capacitor placement significantly exacerbated harmonic distortions, which could damage equipment.

The optimization methodology developed in this research successfully identified capacitor locations and sizes that minimized losses and maintained both voltage and harmonic distortion within acceptable limits. The analysis showed that using a single capacitor bank was inadequate for meeting both voltage and harmonic constraints. Conversely, the deployment of two or more optimally placed capacitors led to a 37% reduction in losses relative to the baseline with harmonics, while keeping voltages above 0.95 p.u. and the THD below 5%.

These outcomes affirm the robustness of the proposed optimization framework in determining optimal capacitor placements that balance the critical objectives of reducing losses, regulating voltage, and mitigating harmonic disturbances in distributed networks with renewable energy sources. Ultimately, this research delivers substantial advancements in addressing the complexities of capacitor placement in modern distribution grids amid growing DG penetration and power electronic loads, offering network operators a viable, efficient, and reliable solution to improve system performance, efficiency, and quality.

Table 6. Comparison of simulation results with the results of the reference [25].

Results	**Proposed method**		**Reference [25]**	
	Before Capacitor Placement	**After Capacitor Placement**	**Before Capacitor Placement**	**After Capacitor Placement**
$\boldsymbol{P_{Loss}}(\boldsymbol{KW})$	518	325	452	250
$\boldsymbol{THD_{max}}(\%)$	10	4.8	7.41	4.98
$\boldsymbol{V_{max}}(\boldsymbol{pu})$	1.05	1.05	1.05	1.0500
$\boldsymbol{V_{min}}(\boldsymbol{pu})$	0.88	0.95	0.957	0.992

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Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper. The ethical issues, including plagiarism, informed consent, misconduct, data fabrication and/or falsification, double publication and/or submission, redundancy, have been completely observed by the authors.

Credit Authorship Contribution Statement

Narges Bagheri: Conceptualization, Software, Roles/Writing - original draft. **Mohammad Amin Bahramian:** Resources, Roles/Writing - original draft. **Ali Asghar Ghadimi:** Conceptualization, Formal analysis, Methodology, Roles/Writing - original draft.

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